REMARKS

A new, more descriptive title has been submitted.

The indication of the allowability of Claims 4-8 is noted with appreciation.

The rejection of Claims 1-3 as being anticipated by Lamberg, et al. under 35 U.S.C. §102 (b) is, however, traversed, and reconsideration is respectfully requested.

Initially, Applicants note the change of "backward" to --forward-- direction in Claim 1 consistent with their description at page 9, lines 22-26 relating to what occurs at power cut-off.

Next, Applicants note the reference to devices (M3, M2, D3) in the Lamberg, et al. publication. But no M3 device is disclosed in this publication. Paragraph [0025] refers only to switches M1 and M2, the latter's base being driven by diode D2 high.

Applicants attach a comparison chart showing their invention in relation to the Lamberg et al. circuit, including their equivalent circuits. From this chart, it becomes readily apparent what the salient differences between the two circuits are.

In particular, the MOS1 and MOS2 transistors in the application drawings are designated by numerals 3 and 4 on the attached chart (left-hand side). These are P-type MOS transistors configured such that they constitute two diodes at power cut off and are connected with a forward direction as viewed from the direction of the digital circuit (numeral 8 in the chart) toward the power supply terminals (numerals 1 and 2). When the power is cut off, the voltage V2 supplied to the digital circuit is kept at 2Vd which is about 1.2V which corresponds to two diodes each having a forward voltage Vd, notwithstanding that the voltage V1 between the power supply terminals becomes zero. The voltage V2 allows the digital circuit to be operated as being constituted by flip-flops and RAM. This means that the information stored in the flip-flops and RAM inside the digital circuit is maintained.

The Lamberg et al. circuit uses a voltage-supply switch M1 with which the diode D3 are connected in a backward direction to prevent back flow to the power source. Rather than forming a backup, these diodes serve to prevent a backward flow to the power source. As described at paragraph [0026], when a message to assume the zero-power mode is received, the gate control voltage of the switch M1 is caused to fall, thereby turning that switch off. The circuit electronics 6, 7 is disconnected from the power supply as a result. This is not an anticipatory teaching of the claimed backup circuit of the present invention.

Accordingly, early and favorable action is now earnestly solicited.

If there are any questions regarding this amendment or the application in general, a telephone call to the undersigned would be appreciated since this should expedite the prosecution of the application for all concerned.

If necessary to effect a timely response, this paper should be considered as a petition for an Extension of Time sufficient to effect a timely response, and please charge any deficiency in fees or credit any overpayments to Deposit Account No. 05-1323 (Docket #056205.57291US).

Respectfully submitted,

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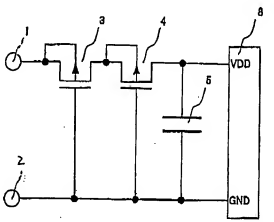
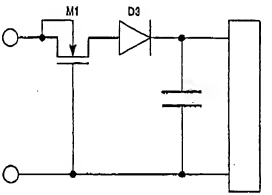
	Present Invention	Lamberg (US 200/90120)
Basic Circuit		
Devices	Tr 3: P-type MOS Tr 4: P-type Mos	M1: N-type MOS D3: Diode
Equv. Circuit